

Intrinsity Announces 2 GHz FastMATH Adaptive Signal Processor and FastMIPS Microprocessor for Embedded Systems; Embedded Processor Forum 2002

-- *Business Wire*, 4/22/2002

New Adaptive Signal Processor(TM) Chip Provides ASIC-Level Computational Performance with the Programming Advantages of Embedded Microprocessors

Intrinsity, Inc. a fabless semiconductor company, today announced the FastMATH(TM) microprocessor, a multi-GHz Adaptive Signal Processor(TM) chip that delivers unsurpassed programmable performance on real-time, adaptive signal processing applications.

Intrinsity's FastMATH(TM) microprocessor combines an innovative MIPS(R)-based architecture with 2 GHz speeds, delivering unprecedented real-time signal-processing performance in applications that would otherwise require banks of DSPs, expensive FPGAs or power-hungry desktop CPUs. Unlike those products or exotic alternatives, the FastMATH(TM) microprocessor is fully-programmable, scaleable and uses industry-standard development tools.

The price-performance and programming ease of Intrinsity's FastMATH(TM) microprocessor improves the economics and time-to-market schedules of many application areas, including medical imaging, military systems, network infrastructure and mobile data communications. Designed to scale beyond 4 GHz, the FastMATH(TM) processor delivers six times the performance of the fastest DSPs on common, math-intensive operations, such as the Fast Fourier Transform (FFT) algorithm. Adaptive signal processing algorithms are even more math-intensive and must quickly compute new system parameters based on multiple high-speed data streams.

"DSPs, FPGAs and desktop processors are clearly not meeting all the needs of today's high-performance adaptive signal processing applications. Intrinsity is utilizing its patented design technology, Fast14(TM) Technology, to create very high performance processors that will help our customers accelerate the wide-spread adoption of these applications," stated Paul Nixon, CEO, president and co-founder of Intrinsity. "Our FastMATH(TM) Adaptive Signal Processor(TM) product can provide the computational speed of ASICs, while delivering the well-proven cost and time-to-market benefits of industry-standard RISC microprocessors."

Adaptive signal processing systems typically consist of arrays of changing data that require complex processing to deliver real-time performance in response to changing conditions. Broadly-defined examples include picking signals out of background noise, canceling out interference from multiple sources and dynamically altering systems to respond to inputs from sensors or data streams. A large number of well-established adaptive signal processing algorithms already demand either higher computation rates or lower-cost implementations - or both.

The FastMATH(TM) Adaptive Signal Processor(TM) product has integrated on one piece of silicon three key components designed to meet these challenging conditions:

-- 2 GHz Matrix and Parallel Vector Math Unit - Provides exceptional parallel data computational performance on the commonly-used matrix and vector math data types found in adaptive algorithms.

-- 2 GHz MIPS32(TM) Processing Core - Provides the ease of programming and flexibility to address changing algorithms and standards.

-- High-Speed I/O - Allows complex, adaptive algorithms to be partitioned cost-effectively across multiple FastMATH(TM) processors by providing dual RapidIO(TM) ports.

For the first time, these elements are combined to form an Adaptive Signal Processor(TM) chip capable of delivering unprecedented programmable performance in real-time signal processing applications. This technology is especially valuable to designers of wireless systems as they innovate new ways to extend the capacity of cell towers in wireless systems:

"As more users crowd the usable radio spectrum and demand higher data rates, more complex processing is required to make efficient use of this limited resource," stated Dr. Jim Gunn, Forward Concepts Senior Consultant. "By accelerating adaptive signal processing algorithms with their multi-GHz FastMATH(TM) processor, Intrinsicity offers technology that can enable wireless systems to make more efficient use of the limited bandwidth available for each cell site."

Multi-user detection (MUD) is an example of an emerging solution to cell site capacity limitations. "Intrinsicity's FastMATH processor provides a compelling, highly scalable solution to the intensive math computational needs of the MUD algorithms," said Barry Isenstein, VP & General Manager of Mercury Computer Systems' Wireless Communications Group.

Intrinsicity also announced today the 2 GHz FastMIPS(TM) high-performance MIPS-based(TM) embedded processor. Delivered from a standard 0.13-micron foundry process and scaleable to 4 GHz, the FastMIPS(TM) product benefits from Intrinsicity's Fast14(TM) Technology to allow multi-GHz performance without exotic manufacturing techniques. Targeted at high-performance embedded applications, the FastMIPS(TM) product also includes dual-RapidIO(TM) ports to enable balanced system performance.

Intrinsicity is a MIPS architectural licensee, and the FastMATH(TM) and FastMIPS(TM) processors are based on the MIPS32 ISA. The selection of the MIPS architecture makes designs easy-to-implement, allowing customers to use best-of-breed design tools from suppliers such as Corelis, Green Hills Software, HelloSoft, OSE Systems and WindRiver.

"We are excited to announce that Green Hills' award-winning Multi software development environment will support Intrinsicity's embedded solutions," said Craig Franklin, Green Hills Software's Vice President of Advanced Products, Inc. "We recognize that the FastMIPS and FastMATH processors provide industry-leading performance for both wireline and wireless applications. Customers developing software for these processors will benefit from the rich feature-set and debug capabilities of Multi, the number one development tools environment for MIPS-compatible processors."

"We are pleased that Intrinsicity has chosen the MIPS architecture as a key facet of its development strategy," said John Bourgoin, chairman and CEO of MIPS Technologies. "Intrinsicity's and MIPS' licensing agreement will open up new markets and increase the number of growth opportunities for both companies."

Intrinsicity will begin sampling its FastMATH and FastMIPS processors in 4Q 2002. Additional details will be disclosed at the Embedded Processor Forum that begins on April 29, 2002. Complete product specifications are available with the completion of a non-disclosure agreement.

About Intrinsicity:

Intrinsicity, Inc. is a fabless semiconductor company enabling the creation of more powerful, real-time and intelligent embedded systems. Founded in May 1997 with headquarters in Austin, Texas, and offices in Boston and Tokyo, Intrinsicity has more than 80 employees with more than nine centuries of cumulative processor design experience. For more information about the company visit its Web site at www.intrinsicity.com.

About MIPS Technologies

MIPS Technologies, Inc. is a leading provider of industry-standard processor architectures and cores for digital consumer and network applications. The company drives the broadest architectural alliance that is delivering 32- and 64-bit embedded RISC solutions. The company licenses its intellectual property to semiconductor companies, ASIC developers and system OEMs. MIPS Technologies and its licensees offer the widest range of robust, scalable processors in standard, custom, semi-custom and application-specific products. The company is based in Mountain View, Calif., and can be reached at 650/567-5000 or www.mips.com.

INTRINSITY, FAST14 and FASTMATH are trademarks of Intrinsicity, Inc. MIPS is a registered trademark and MIPS32, MIPS-based and FASTMIPS are trademarks of MIPS Technologies, Inc. RAPIDIO is a trademark of RapidIO Trade Association. All other trademarks are for reference purposes only and are the property of their respective owners.

CONTACT:

Shelton, Dallas

Katie Olivier, 972/239-5119

kolivier@sheltongroup.com

URL: <http://www.businesswire.com>