



Solving the multiprocessor design problem for wireless LANS

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Wireless LANs (WLANs) are emerging as a technology that is attracting considerable interest from potential users and an expanding vendor community. However, until recently, its benefits have not been fully realised due to inadequate wireless standards, slow data rates, lack of interoperability among vendors, and excessive costs. New driving forces such as the availability of developing standards and new sources of critical design building blocks, eg, high performance DSP cores and software need to be supported by a specialist WLAN design environment. Here BOPS Inc describe their approach to WLAN design and its associated tools and components.

Commercially significant high-speed WLAN standards are emerging in two international standards organisations. First, the US-centric IEEE has the 802 LAN/MAN standards committee that develops Local Area Network (LAN) and Metropolitan Area Network (MAN) standards. The 802.11 working group with responsibility for WLAN standards has two standards: 802.11b (2.4 GHz) and 802.11a (5 GHz). The 802.16 standard addresses fixed broadband wireless access applications.

Second, European-centric ETSI has the BRAN (Broadband Radio Access Networks) project that has responsibility for HiperLAN/2 (5GHz). The 802.11a and HiperLAN/2 are competing standards that share an essentially common PHY (physical layer) but differ in their MAC (media access control) protocol. Table 1 summarises these standards. These standards operate in license exempt (or unlicensed) bands, with comparable 2.4GHz and 5GHz frequency allocations worldwide. Licensed operations in other, typically higher frequency, bands are defined for fixed wireless services (LMDS, MMDS) based on IEEE 802.16 standards and use similar baseband modulation formats.

Three major WLAN market segments are emerging: consumer or home; enterprise; and public. The consumer or home market enables the use of wireless home networks that connect to the Internet via a single dial-up, high-speed cable modem, or high speed DSL access link. The enterprise segment provides WLAN to address portability within the workplace as well as reduce the reconfiguring costs associated with reorganisations and moves. The public segment provides users with network access by subscription in public places such as airports, hotels, convention centres, arenas, coffee shops and cafes, etc. WLAN equipment includes access points (APs) and a variety of subscriber terminal options. The access point (AP) is the transceiver with which multiple subscriber terminals wirelessly communicate. An AP typically provides access to the Internet or, in the case of Enterprise deployments, to the corporate network. Typical subscriber terminals include PCs, laptops, PDAs, and emerging data-ready cellular phones.

Interestingly, some industry pundits are claiming that WLAN might significantly compete with and take market share from the more highly visible commercial cellular industry's 3G data initiatives. Others envision a more conciliatory environment with the 3G data and WLAN initiatives complementing each other, providing expanded, more complete wireless data solutions, thus fostering a much larger total market. International telecoms consultancy BWCS (UK) forecasts that by 2006 there could be 20 million WLAN equipped computers, laptops, and PDAs and that approximately 17 million of these could be hotspot capable (public places). Further, they forecasted there could be 114,220 hotspots in 2006 (up from 6,300 at YE2001) generating service revenues of US \$7.3 billion.

SOC multiprocessor WLAN solutions

The difficult challenge for WLAN system designers and the vendors with whom they are associated, with severe time-to-market pressures, is the problem of addressing this very attractive, increasingly competitive, emerging market while accommodating evolving requirements that include new and changing standards, and a variety of terminal architectures. To further complicate matters each design variation has different performance and power goals; different terminal and AP requirements, and multiple market segments requirements. The traditional alternatives for implementation have included FPGAs, ASICs, merchant programmable DSPs, RISCs, etc. However, these alternatives have significant deficiencies in areas of power consumption, integration, cost, and especially flexibility. With the current mainstream 0.18 μm and newer 0.13 μm CMOS technology, the long anticipated System-on-Chip (SOC) era offers an excellent new flexible alternative employing SOC multiprocessor WLAN solutions.

The company with which this author is associated, BOPS, Inc. has introduced its Wireless LAN SOC in a Box, which is claimed as the first IP SOC solution that is configurable and interoperable for multiple wireless LAN standards. These LAN standards include: 802.11b (Wi-Fi), 802.11g (TI or Intersil PHY proposals), 802.11a, HiperLAN/2, 802.11x, and Bluetooth. The SOC in a Box includes complete IP system-on-chip solutions that are delivered as pre-packaged application solutions that are foundry independent. It includes system design, hardware designs, peripheral designs, software designs, design services, and foundry services. Importantly, it is highly flexible through customer-specified hardware customisation and pre- and post-manufacture software customisation.

Figure 1 illustrates representative hardware IP that may be integrated on a WLAN baseband SOC solution. The hardware IP required to implement WLAN functions on an SOC include DSP cores for the physical layer (PHY); host controller (RISC) for the Media Access Controller (MAC) functions and general terminal control functions; Application Specific Accelerators; various memory options such as integrated or external SRAM or FLASH; interfaces to the RF and Data Acquisition circuits; and various interfaces to the subscriber terminals or APs.

The applications need optimised, software compatible DSP cores for WLAN standards requiring throughput intensive OFDM modulation for 802.11a and HiperLAN/2 and DSSS processing for 802.11b. These cores provide flexibility to address these standards on a single SOC and to tailor specific AP or terminal requirements with appropriate power, performance, and area targets. Designers may implement circuits with higher clock rates, higher performance, and greater power consumption; or lower clock rates, less performance, and lower power consumption (eg, battery operation). BOPS cores support these trade-offs by providing software implementation of high throughput functions using higher clock rates but with reduced logic. Conversely, applications specific accelerators can be used to reduce clock rate and achieving lower power consumption.

BOPS Open IP license, business & support model

BOPS Intellectual Property (IP) offerings are based on a licensable, ARM or MIPS-like business model that enables OEMs to access multiple competitive sources for DSP, CPU/RISC, interface, and other IP for SOC designs. As a member of the Virtual Socket Industry Association (VSIA), BOPS supports the VSIA stated mission "to dramatically accelerate system chip development by specifying open standards that facilitate the mix and match of Virtual Components from multiple sources." VSIA is defining open standards for the exchange and reuse of IP in SOC designs.

BOPS IP is typically "soft IP" that is defined at the Register- Transfer-Level (RTL) of design and offers the advantages of process and fab independence. Coupled with modern synthesis technology and mainstream 0.18 μm or emerging 0.13 μm CMOS processes, soft IP provides an efficient and flexible strategy to achieve the desired high performance, low power,

high integration, low cost solutions for WLAN products. Selected "hard IP" in GDSII format is available that can further reduce development cycle time if process flexibility is not a major consideration.

The open IP business model changes the design task from a comparatively simpler but restrictive chip purchase and board design to a more flexible IP-centric model that includes IP licensing agreements usually with upfront fees and chip royalties. Because the IP space is broad and complex, multiple IP sources will routinely be integrated in a chip design to develop highly optimised differentiated solutions. For WLAN applications this potentially could include BOPS WLAN DSP IP, ARM or MIPS IP, various interface and memory IP, as well as customer IP.

The resources for SOC development may exceed the internal abilities and skills sets of some organisations and may be further exacerbated by extreme time-to-market pressures. Creative and flexible partnerships are an essential business model in this environment. Specific development teams will be rapidly formed with members from multiple organisations. The required IP and skill sets include application and system engineering, chip design and layout, design services, EDA tools and services, software, hardware, test, foundry, etc. These requirements have been recognised and a network of alliance partners and TopStar authorised design centres to address these issues have been created. The Wireless LAN team includes Tality Corp. for SOC and related design services; HelloSoft, Inc. for WLAN application and software IP and expertise; Fraunhofer Institute for Integrated Circuits, Applied Electronics, for hardware IP and design services; TSMC and UMC for foundry and process technology services, plus many others. In association with its partners BOPS are able to provide a full set of system element Intellectual Property required for flexible, efficient, and cost effective WLAN SOC implementations.

WLAN SOC design environment, & support tools

A complete integrated design environment, as presented in figure 2, enables designers to quickly realise the desired SOC solution starting with the high level concept. One of the most important areas of development for a complex, multiprocessor SOC is the availability and support of the models and development tools to efficiently and accurately perform the necessary feature trade-off and system partitioning in the early design stage. BOPS supports a comprehensive environment for architecture and design space exploration to facilitate the development of final SOC specification that meets the required design targets. The actual SOC design can then be implemented with confidence by the hardware and software development teams in parallel to minimise the development time while verifying design correctness at each successive development stage with appropriate test benches. BOPS supplied IP and tools are generally depicted on the left and include pre-verified RTL IP as well as a complete suite of hardware and software design tools. These tools integrate with customer's existing IP, chip design tools, and host software tools. Customers essentially utilise their familiar design environment supplemented by BOPS as well as required 3rd party tools. BOPS tools integrate with all major EDA vendor tools. On the right of figure 2 are BOPS DSP software developments tools.

Considerable resources are devoted to ongoing development efforts to provide a suite of tools to create an integrated and efficient design environment that facilitates a shortened design cycle. The suite of tools includes a software development kit (SDK) and several supporting boards.

The Software Development Kit (SDK) is a growing development toolbox that tightly integrates tools for the application software programmer, the SOC designer, the firmware designer, and the system architect into a single development environment. The SDK integrates compiler, assembler, linker, loader, debugger and simulator tools into a seamless environment for DSP application development, and allows customers to convert C files quickly and efficiently into BOPS ManArray assembly code for their DSP applications. The Halo C parallelising compiler facilitates efficient DSP code development that takes full advantage of the architecture's three

levels of parallelism and provides for flexible control and manual intervention for customised C or assembly code insertion for time- critical code.

The Jordan Evaluation Board is a PCI software development platform designed to speed the development of software for a variety of evolving communications, multimedia and Wireless applications. The card contains a BOPS Manta DSP chip and a MIPS QED RISC processor. The Manta chip has a BOPS 2x2 DSP core containing three BOPS PEs (processing element) and a single SP/PE (sequence processor/PE) parallel DSP processing elements and its single-cycle cluster switch. The chip also contains a 32bit PCI bus, 64bit SDRAM, and 32bit MIPS SysAD bus. The board has 64Mbytes of 100 MHz SDRAM, 32bit PCI 2.1 Bus and form factor, and EIA-232 serial port. The board provides full BOPS SDK support.

The Travis Prototyping Board provides a hardware and software prototyping platform for real-time, high-speed evaluation of the system elements of a SOC utilising BOPS scalable ManArray architecture cores. Like the Jordan board, the Travis board also contains a BOPS Manta chip. Additionally, it includes a large uncommitted Xilinx FPGA for other customer-specific logic. It also has the 32bit PCI 2.1 bus and connector, 148-pin daughter board for prototyping application specific functions and logic, and 400 I/O expansion pins for off board cabling. The board allows customers to quickly build custom prototypes by adding various functions through add in ports, ARM host daughter card, and large physical and logic space.

The Xemulator Board provides a complete emulation of the entire SOC being developed before it is released for fabrication. The board provides hardware emulation of the specific application processor that is an optimised subset of the proven ManArray architecture. The board provides FPGA emulation of the ManArray processor that can be tailored to accommodate application requirements such as bus width, bus protocols, and external interfaces. Instruction set additions can also be emulated. Like the Jordan and Travis boards it maintains the standard microcontroller host(s), PCI bus interface, and other peripherals.

Traditional board designs included multiple chips for various functions such as baseband DSP, host microcontroller, application specific accelerators (eg, ASIC, FPGA), and various interface and memory circuits. While the designers could implement system level solutions, the inherent restrictions of fixed components naturally limited the level of optimisation possible with respect to features, performance, power and cost.

The powerful combination of current generation of process technology, availability of optimal cores, and improved design implementation methodology and tools now makes it possible for designers to achieve higher degrees of innovation through integrated solutions that deliver manageable development time and risk. The current generation of mainstream 0.18 micro m and newer 0.13 micro m CMOS technology available from leading independent fabs can deliver economical solutions for very high levels of integration. Availability of optimised, openly licensable IP cores and improved design flows and tools enable new levels of optimised integrated solutions.

Tel: 001 650 254 2800

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